1   1.   A system for recovering and aligning synchronous data transmissions,
2   comprising:
3   a transmitter configured to transmit a source clock signal and a plurality of
4   data groups over a plurality of channels, the plurality of data groups being transmitted during
5   the same clock cycle pursuant to the source clock signal, each data group being transmitted
6   over a corresponding channel; and
7   a receiver configured to receive the source clock signal and the plurality of
8   data groups over the plurality of channels, the receiver further configured to include:
9   for each channel: (a) a local clock configured to generate a local clock
10   signal based on the source clock signal, the local clock signal being phase-shifted from the
11   source clock signal by a predetermined amount of phase shift, (b) a logic device configured to
12   clock in the data group received over the channel using the local clock signal, (c) a sequence
13   number generator configured to generate a sequence number associated with the data group,
14   (d) a FIFO buffer configured to store and output the clocked-in data group and the associated
15   sequence number, (e) a memory device configured to store the clocked-in data group from
16   the FIFO buffer using the associated sequence number as a memory address, the memory
17   device further configured to output a predetermined portion of its contents after a
18   predetermined capacity threshold is reached.

1   2.   The system of claim 1 wherein the transmitter is further configured to
2   transmit a start-of-cell signal to the receiver; and
3   wherein upon the receiver detecting the start-of-cell signal having a specific
4   value for a predetermined cycle period, the sequence number generators are synchronized.

1   3.   The system of claim 1 wherein the receiver is implemented using a
2   plurality of field programmable gate arrays.

1   4.   The system of claim 3 wherein the local clock is implemented using a
2   digital clock manager associated with a field programmable gate array.

1   5.   The system of claim 1 wherein the predetermined amount of phase
2   shift is determined empirically.

1   6.   The system of claim 1 wherein the predetermined amount of phase
2 shift is calculated based on respective latency delays of the source clock signal and a
3 corresponding channel.

1   7.   The system of claim 1 wherein each data group includes a plurality of
2 data signals; and
3   wherein the plurality of data signals within each data group have the same
4 latency delay over the corresponding channel.

1   8.   The system of claim 1 wherein the memory device is a dual port
2 random access memory.

1   9.   The system of claim 1 wherein the sequence number generator is
2 incremented every clock cycle pursuant to the local clock signal.

1   10.   A backplane incorporating the system as recited in claim 1.

1   11.   A system for recovering and aligning synchronous data transmissions,
2 comprising:
3   a transmitter configured to transmit a source clock signal and a plurality of
4 data groups of over a plurality of channels, wherein a set of data groups collectively forming
5 a data word is transmitted during each clock cycle pursuant to the source clock signal, each
6 data group in the set of data groups being transmitted over a corresponding channel; and
7   a receiver configured to receive the source clock signal and sets of data groups
8 over corresponding channels, the receiver including:
9   a plurality of local clocks, each local clock configured to generate a
10 local clock signal based on the source clock signal, the local clock signal being phase-shifted
11 from the source clock signal by a predetermined amount of phase shift;
12   a plurality of devices, each device configured to receive and clock in
13 corresponding data groups from a corresponding channel using the local clock signal from a
14 corresponding local clock;
15   a plurality of sequence number counters, each sequence number
16 counter associated with a corresponding device and configured to provide respective
17 sequence numbers for data groups received by the corresponding device;

18   a plurality of buffers, each buffer configured to store and output

19   clocked-in data groups from a corresponding device and their associated sequence numbers;

20   and

21   a plurality of memory devices, each memory device configured to store

22   the clocked-in data groups from a corresponding buffer using their associated sequence

23   numbers as memory addresses, each memory device further configured to output a

24   predetermined portion of its contents after a predetermined capacity threshold is reached.

1   12 .   The system of claim 11 wherein the transmitter is further configured to

2   transmit a start-of-cell signal to the receiver; and

3   wherein upon the receiver detecting the start-of-cell signal having a specific

4   value for a predetermined cycle period, the sequence number counters are synchronized.

1   13.   The system of claim 11 wherein the receiver is implemented using a

2   plurality of field programmable gate arrays.

1   14.   The system of claim 13 wherein the local clocks are implemented

2   using two or more digital clock managers associated with plurality of field programmable

3   gate arrays.

1   15.   The system of claim 11 wherein the predetermined amount of phase

2   shift associated with each local clock is determined empirically.

1   16.   The system of claim 11 wherein the predetermined amount of phase

2   shift associated with each local clock is calculated based on respective latency delays of the

3   source clock signal and a corresponding channel.

1   17.   The system of claim 11 wherein each data group includes a plurality of

2   data signals; and

3   wherein the plurality of data signals within each group have the same latency

4   delay over the corresponding channel.

1   18.   The system of claim 11 wherein the plurality of memory devices

2   include a dual port random access memory.

1   19.   The system of claim 11 wherein each sequence number generator is

2 incremented every clock cycle pursuant to the local clock signal associated with a

3 corresponding local clock.

1   20.   A backplane incorporating the system as recited in claim 11.

1   21.   A method for recovering and aligning synchronous data transmissions,

2 comprising:

3   transmitting a source clock signal and a plurality of data groups from a

4 transmitter to a receiver per clock cycle pursuant to the source clock signal, the plurality of

5 data groups collectively forming a data word;

6   at the receiver:

7   using the source clock signal to create a plurality of local clock signals,

8 each local clock signal being phase-shifted from the source clock signal by a corresponding

9 predetermined amount of phase shift;

10   clocking in each data group using a corresponding local clock signal;

11   assigning a sequence number to each clocked-in data group;

12   storing each clocked-in data group and its assigned sequence number

13 in a corresponding buffer;

14   reading out each clocked-in data group and its assigned sequence

15 number from its corresponding buffer; and

16   storing each read-out data group into a corresponding dual port

17 memory using the assigned sequence as its memory address.

1   22.   The method of claim 21 further comprising:

2   sending a special start-of-cell signal and an alignment cell from the transmitter

3 to the receiver;

4   at the receiver, upon detecting the special start-of-cell signal, initializing

5 sequence numbers to be assigned to clocked-in data groups to a starting value, the starting

6 value being embedded in the alignment cell.

1   23.   The method of claim 21 further comprising:

2   at the receiver, incrementing the sequence number for future assignment to a

3 next clocked-in data group.

1   24.   The method of claim 21 further comprising:

2   at the receiver, reading out a predetermined portion of each dual port memory.

1   25.   The method of claim 21 wherein the corresponding predetermined

2 amount of phase shift for each local clock signal depends on the respective latency delays of

3 the source clock signal and a corresponding data group.

1   26.   A backplane utilizing the method as recited in claim 21.